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Analysis and Optimization of Power and Area of Domino Full Adder and its Applications

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Abstract: *In this paper we analyse different domino logic full adder circuits by considering area, power consumption and number of transistors as the three main parameters which plays an important role in digital design. We proposed a hybrid logic based domino full adder circuit which provides better performance in the above mentioned three parameters than the existing circuits. The two important applications of full adder 1-bit ALU and 2-bit Comparator of the proposed circuit is also presented. All the circuits are designed and simulated using DSCH and MICROWIND tool.*

Keywords: *Full adder, Domino logic, Area, power consumption, ALU, and Comparator.*

I. Introduction

Low power has become main constrain for portable systems. These systems require more feature and high battery life time. The total power of the electronic circuit is the sum of static power, dynamic power and short circuit power. The dynamic power consumption becomes significant contributor to over all power consumption. Hence, the reduction of power consumption is compulsory.

After studying various techniques in literature found that domino circuits require less power consumption than static circuits. The operation of domino circuits is based on charging and discharging of output node capacitance. These circuits are applied for higher speed of the system. XOR cell is essential to drive various digital circuits such as adder, comparator, multiplier, parity bit generator and checker circuit etc.

Full adder is the foundation element of complex arithmetic circuits like addition, multiplication, division, exponent circuits. Thus, enhancement of the performance of the adder block directs to the improvement of the overall system performance. Hence many researchers are now working to make full adder circuits to make it faster adder cell with smaller area and consuming smaller area.

A 1-bit full adder adds three single-bit numbers, often written as A, B, and Cin. The A and B used as operands and Cin bit are carried in from the succeeding least significant stage. Adder circuits produce double-bit output, carry-out and sum typically represented by the signals Cout and Sum, where

$$Sum = A \text{ xor } (B \text{ xor } Cin)$$
$$Cout = A.B + A.Cin + B.Cin$$

This paper is prepared as follows. Section II realizes the existing methods. The proposed full adder, 1-bit ALU and 2-bit comparator are analyzed in section III. In section IV we have shown the proposed circuit simulation for power and area, and the results are analyzed and compared with previous proposed work. Section V of the paper concludes the work.

II. Existing Methods

The selection of a logic design style is inclined to a number of factors namely layout area, speed of circuit and power dissipation, process technology, and used supply voltage etc. While dynamic circuits can be used to implement high-speed logic gates, there are anxieties over leakage currents and high power dissipation. Hence, in this section we analyse and compare different existing full adders like SCMOS, SFLDA, SFDA, DRDFA, and HSDFA among them as follows:

A. Conventional Static Cmos Full Adder

The conventional static CMOS full adder cell (36T) is shown in below Fig.1.consists of Pull-Up and Pull-Down networks. The PMOS transistors in Pull-Up network is the dual network of the NMOS Transistors in Pull-Down network. The - sign on input terminals indicates the complementary signals. The advantage of CMOS logic is that it dissipates less dynamic power. The disadvantage of static CMOS logic is the higher propagation delays and requires 2n transistors where n is the number of inputs and larger chip area and also suffers with low fan-out capability.

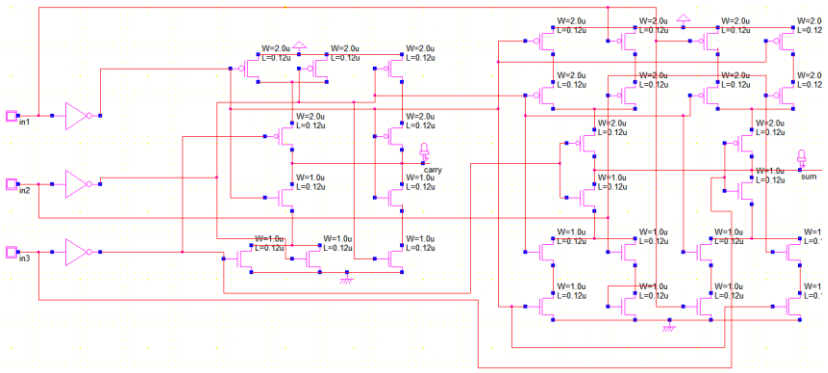

Fig.1.The Schematic Diagram of a 1-bit Static CMOS full adder cell

To overcome the drawback of static cmos full adder we go for dynamic cmos logic which is offers smaller area by reducing number.of.transistors as said earlier. But the drawback of Dynamic logic circuits is more power consumption and slower speed. One of the popular implementation of dynamic logic is domino logic.

B.Concept of Domino Logic

Domino logic is a CMOS-based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. It allows a rail-to-rail logic swing. The Dynamic Domino, circuits operate using a sequence of pre-charge and evaluation phases orchestrated by the system clock signal as in Fig.2. The domino logic involves the implementation of only the nMOS logic as compared to the static cmos circuits in PDN due to which there is colossal amount of reduction in the number of transistors in domino logic thus reducing the area of the circuit.

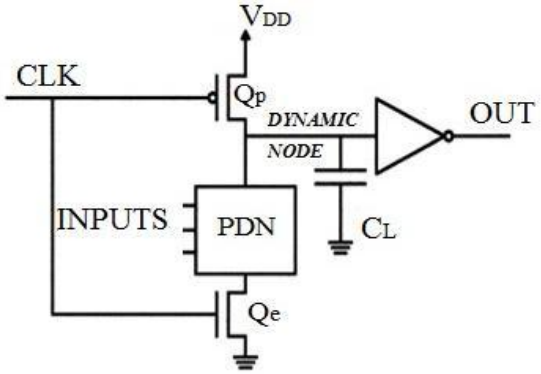

Fig.2. Basic Domino Circuit

In the above figure CL represents the parasitic capacitance and PDN represents the pull down network which realizes the logic function to be implemented. When the clock is low the circuit is in precharge phase and Qp is on and Qe is off. The dynamic node precharges to Vdd and the output of the cmos inverter is low. When clk =1 the circuit is in evaluation phase, Qe is on and Qp is off.

When the input combination result in logic '0' then the dynamic node stays charged and output is low. When the input combination results in logic '1' then the dynamic node are discharged to ground and the output of the cmos inverter is high. However these domino logic gates suffer from lesser noise immunity and higher power dissipation. As the technology scales down the leakage current increases and plays a vital role in the total power dissipation.

C.Standard Footless Domino Logic Full Adder

The footless scheme is characterized by the fact that discharge of dynamic node is faster. This property is exploited by the high-performance circuits. The circuit of the SFLD logic is shown in Fig.3. Operation of Footless-Domino is as follows: During the pre-charge phase, i.e. when then clock (CLK) is LOW, the dynamic node is charged to VDD and the keeper transistor turns ON to maintain the voltage of the dynamic node.

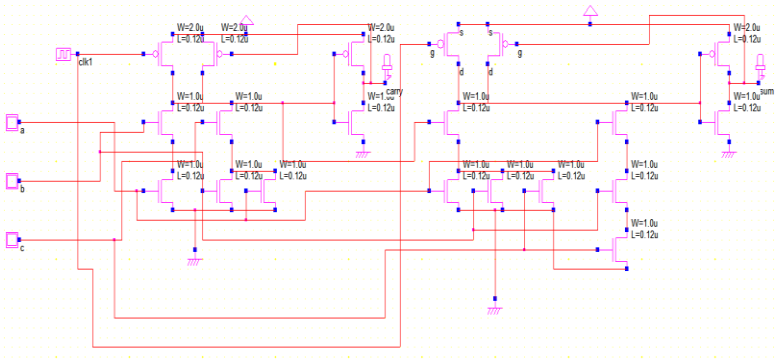

Fig.3.Standard Footless Domino logic full adder

During the evaluation mode, i.e. when the CLK goes HIGH, the dynamic node is either discharged to ground or remains HIGH depending on the inputs. But the circuit suffers with large amount of power dissipation.

D. Standard Footed Domino Logic Full Adder

The footer nMOS transistor is connected to the source of evaluation nMOS transistor to obtain the FDL design which basically reduces the leakage current.Fig.4 shows the most conventional footed domino logic circuit. When clock is low, the dynamic node is pre-charged to VDD. In this phase the footed transistor is turned off, which reduces the leakage current. When clock goes high, footer transistor is turned on. So, depending on incoming data to pull-down network the state of output node is obtained.

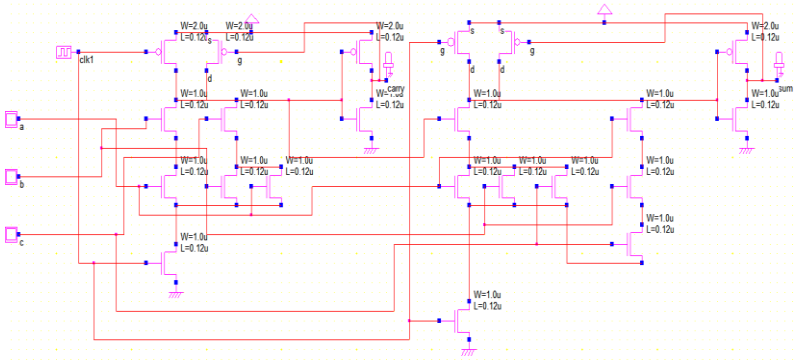

Fig.4. Standard footed domino logic full adder

This footed circuit offers better power consumption with slower speed and the no. of transistors is also increases than the previous circuit.

E.Dual Rail Domino Logic Full Adder

Dynamic domino gates have the severe limitation of not being able to implement inverting logic functions (such as NOR, NAND, XOR) and high power consumption due to clock. Dual-Rail Domino Logic is a precharged circuit technique which is used to improve the speed of CMOS circuits.Fig.5.shows a Dual-Rail Domino full adder cell. A domino gate consists of a dynamic CMOS circuit followed by a static CMOS buffer.

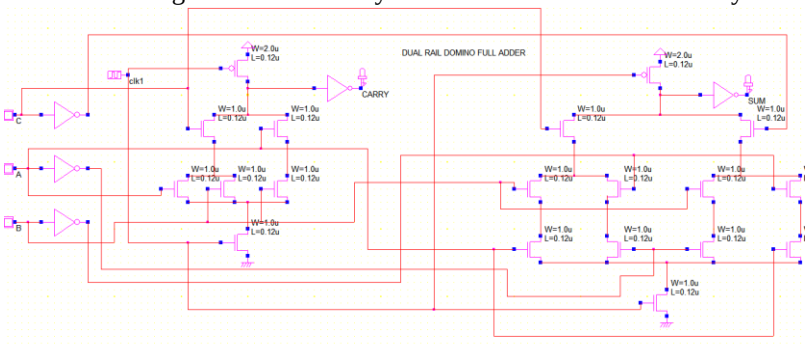

Fig.5.Dual rail domino full adder

One major advantage of the dynamic, precharged design styles over the static styles is that they eliminate the spurious transitions and the corresponding power dissipation. However, in dynamic circuits, additional power is dissipated by the distribution network and the drivers of the clock signal. This circuit offers minimal power consumption and area than the previous circuits but the drawback is it requires more no .of transistors.

F.High Speed Domino Logic Full Adder (Hs)

The circuit of the HS Domino logic full adder is shown in Fig.6. In HS domino the keeper transistor is driven by a combination of the output node and a delayed clock. The circuit works as follows: At the start of the evaluation phase, when clock is high, MP3 and MP6 turns on and then the keeper transistors MP2 and MP5 turns OFF. In this way, the contention between evaluation network and keeper transistor is reduced by turning off the keeper transistors at the beginning of evaluation mode.

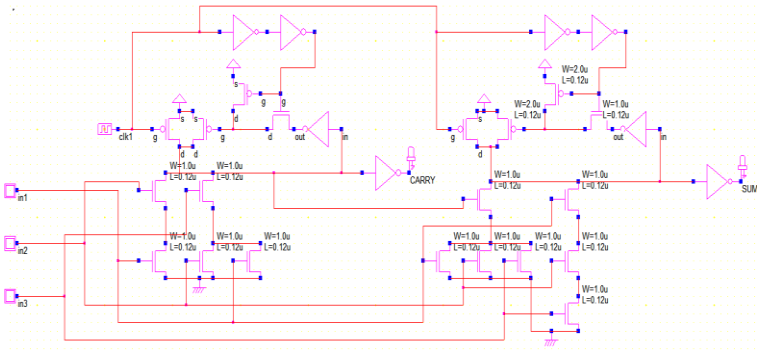

Fig.6. High speed domino full adder

At this moment, if the dynamic node has been discharged to ground, i.e. if any input goes high, the nMOS transistors MN1 and MN2 remains OFF. On the other hand, if the dynamic node remains high during the evaluation phase, MN1 and MN2 turns on and pulls the gates of the keeper transistors. Thus keeper transistors will turn on to keep the dynamic node high, fighting the effects of leakage. It requires more no. of transistors than previous domino adders, but provides less power consumption and better area.

III. Proposed Domino Full Adder

To remove drawbacks of existing domino full adder circuits an efficient design of domino full adder is proposed in this section. The design technique of proposed full adder is as shown in below Fig.7.This proposed adder is designed using hybrid domino xor cell and two 2x1 multiplexers.

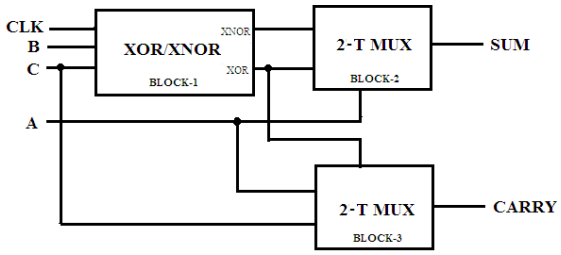

Fig.7. Design technique of Full Adder

The expression of full adder is follows:
SUM = Ā (B xor C) + A (B xnor C) (1)
CARRY = AB + BC + CA. (2)
Equation (1) and (2) show the logical expression of full adder for SUM and CARRY.
The operation of full adder is to add three binary bits. It takes three input signals A, B, Cin and gives two output signals SUM and CARRY. Fig. 7 shows one design technique of full adder. It consists of 3 blocks which are described as follows:
a) First block takes two input signals, clock signal and gives two output signals. It performs XOR and XNOR operation on inputs B and C.

b) Second block is designed using 2T multiplexer. It consists of one nMOS and one pMOS transistor. It has two input signals and one selection line. The output signals of first block act as input signals to this block. This block is designed for the expression shown in Eq. (1). Here A is selection line and XOR and XNOR are two inputs respectively from first block. If A is 0 then XOR logic is the output otherwise XNOR logic.

c) Third block is also designed using 2T multiplexer and it follows the expression shown in Equation (2). It has A, C as input signals and output of XOR as selection line. If XOR signal is 0 then output follows signal C otherwise signal A at output.

The pull down network of the xor cell is designed by both pMOS and nMOS transistors formed as a hybrid network as shown in Fig.8.Here, nMOS keeper transistor is used instead of pMOS to increase the speed of circuit. Two nMOS transistors are connected at dynamic node to give high logic at dynamic node and low logic at output node in evaluation phase. This circuit does not require extra inverters to invert input signals. The drain of P7 and N10 are connected to source of N8. The source of P7 is connected to ground and source of N10 is connected to dynamic node. The drain of P8 and N11 are connected to P6 the source of P8 is connected to ground and the source of N11 is connected to input signal C.

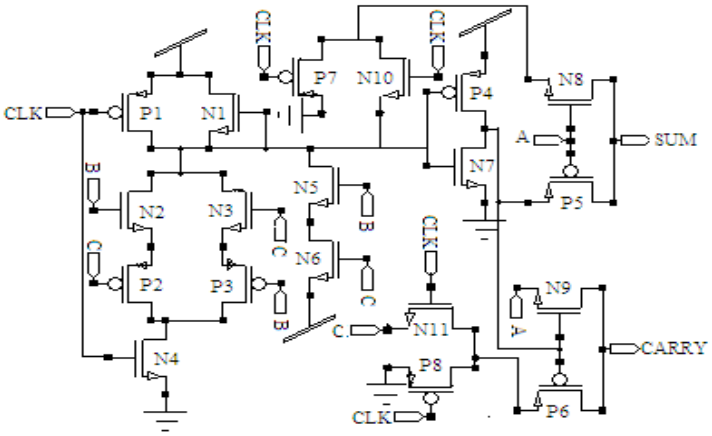

Fig.8**.** Proposed 1-Bit Domino Full Adder.

The operation of this circuit is as follows: When clock signal is low i.e. in precharge phase, transistors P1, P7 and P8 are turn on. This gives low logic at the output of XOR cell and at the source of P6, N8. Therefore, this circuit gives low logic at SUM and CARRY. When clock signal is high i.e. in evaluation phase N4, N10 and N11 transistors are turned on. In this phase, the output of proposed design depends on input signals. For first MUX input signal A acts as a selection line. If A is 0: P5 turns on then XOR output selects for SUM. If A is 1 then N8 XNOR output selects for SUM. For second MUX output of XOR gate act as a selection line. If B XOR C is 0 then C selects as an output of CARRY. If B XOR C is 1 then A acts as an output of CARRY. By adding transistor, a new circuit is obtained that exhibits better performance. Thus, the proposed design works properly for both active high and active low clock signal. Hence the transistor count and performance of proposed full adder is better than existing domino and static full adders.

As an application of the above mentioned circuit 1-bit alu and 2-bit comparator is proposed as presented below.

Proposed 1 bit – ALU

The digital function that implements the micro-operations on the information stored in registers is commonly called an Arithmetic Logic Unit (ALU). The ALU receives the information from the registers and performs a given operation as specifies by the control. The control unit is made up of 4-1 multiplexer. The design of the ALU involves the designing of the Full Adder circuit. The operation part consists of four kinds of operations listed as follows: and, or, addition and subtraction. The 'and' and 'or' operation are realized by using the basic logic gates. A digital multiplexer made from MOS device selects one of the 4 operations results and directs it to a single output line. The full adder performs the computing function of the ALU. It consists of three inputs and two outputs.

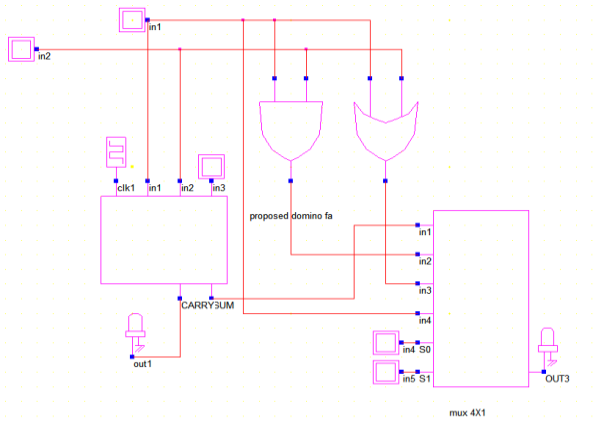

Fig. a. proposed 1-bit ALU

An overall 1 bit ALU is depicted in below Fig. a. The Full Adder will have three inputs and two outputs. The truth table of 1-bit alu is as shown above. The outputs are the Sum and Carry-Out. The Sum is the totalling of A, B, and Cin.

S1	S0	RESULT
0	0	ADD
0	1	AND
1	0	OR
1	1	PASS

Figure: Truth table of 1-bit ALU

The Carry-Out will be used as the input into another ALU when we implement a multi-bit ALU using cascading.ALU will have four different operations, it is required to have two control bits to select which operation is to be performed.

Proposed 2-bit Comparator

In digital system, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number. So comparator is used for this purpose.

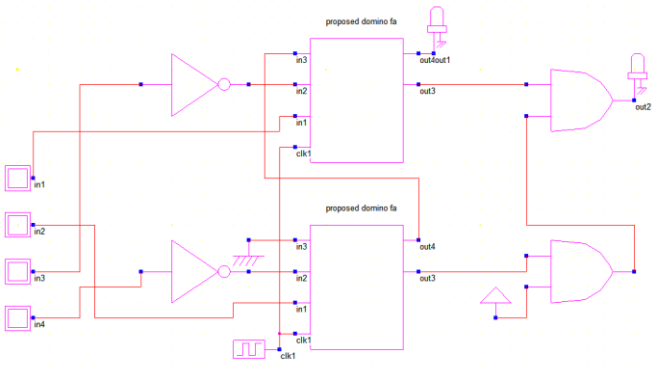

Fig. b. proposed 2-bit comparator

Magnitude comparator is such combinational circuit which compares two numbers say A and B, and then their relative magnitude is determined and outcome specified by three states which indicate whether A>B, A=B and A<B. As said here we design comparator using Full Adder so here we design it as of 2-Bit FA based

comparator consist of full adders, inverters at one of the input and AND gate at the output side with two outputs as shown in Fig. b.

The truth table of 2-bit comparator is as shown below:

A1	A0	B1	B0	B>A	A=B
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	0
A1	A0	B1	B0	B>A	A=B
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	1

Figure: Truth table of 2-bit comparator

IV. Simulation Results

All the above mentioned existing domino full adder circuits and proposed domino full adder, alu and comparator circuits are analysed and simulated at 65nm technology using Dsch and Microwind tool.The obtained results of all the existing and the proposed circuits are as shown in below tables.

Full Adder Type	Area	Power	No. Of Transistors
Footless Domino	31µmx9µm	0.531mw	20
Footed Domino	33µmx10µm	0.306mw	22
High Speed Domino	37µmx10µm	0.215mw	34
Dual Rail Domino	29µmx11µm	10.583µw	29
proposed hybrid domino	30µmx9µm	5.207µw	19
Full Adder Type	**Area**	**Power**	**No. Of Transistors**
Static Cmos	55µmx11µm	19.687µw	36
proposed hybrid domino	30µmx9µm	5.207µw	19

1-Bit Alu Using Full Adder Type	Area	Power
Sfld	44µmx9µm	0.139mw
High Speed Domino	50µm x10 µm	75.387 µw
Sfd	47µmx10µm	70.718µw
Proposed Hybrid Domino	42µmx10µm	5.641µw
1-Bit Alu Using Full Adder Type	**Area**	**Power**
Static Cmos	58µmx11µm	8.903µw
Proposed Hybrid Domino	42µmx10µm	5.641µw

2-Bit Comparator Using Full Adder Type	Area	Power
Sfld	53µmx11µm	0.187mw
High Speed Domino	65µmx12µm	0.140mw
Sfd	57µm x11 µm	57.96µw
Proposed Hybrid Domino	47µmx12µm	9.996 µw
2-Bit Comparator Using Full Adder Type	**Area**	**Power**
Static Cmos	80µmx13µm	12.480µw
Proposed Hybrid Domino	47µmx12µm	9.996 µw

V. Conclusion

In this work both the existing and proposed domino logic full adder circuits are analyzed in terms of area, power consumption and no. of transistors, the simulation results revealed that the proposed full adder circuits offers very low power consumption and smaller area than the above mentioned existing full adder circuits. Also the proposed domino full adder cell based 1-bit ALU and 2-bit comparator showed lower power consumption and area when simulated using Microwind tool. So the proposed circuits are suitable for low power applications with smaller area.

References

[1]. J. M. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits- A Design Perspective", 2nd Prentice Hall, Englewood Cliffs, NJ, 2002.
[2]. J. Uyemura, "CMOS Logic Circuit Design", ISBN 0-7923-8452-0, Kluwer, 1999
[3]. http://en.wikipedia.org/wiki/Adder_(electronics)..
[4]. D. Wang, M. Yang, W. Cheng, X. Guan, Z. Zhu, and Y. Yang, "Novel low power full adder cells in 180nm CMOS technology", IEEE Conference on Industrial Electronics and Applications (ICIEA '09), May 2009, pp. 430–433.
[5]. S. Wairya, R. K. Nagaria, and S. Tiwari, "Performance Analysis of High Speed Hybrid CMOS Full Adder Circuits for Low Voltage VLSI Design", VLSI Design, 2012, pp. 1-18.
[6]. S. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits, Analysis and Design", 2003, Tata McGraw-Hill, New York, NY, USA**.**
[7]. Wang. J, Gong. N, Hou. L, Peng. X, Geng. S and Wu. W, "Low power and high performance dynamic CMOS XOR/XNOR gate design", Microelectronics Engineering, 2011, Vol.88, pp.2781-2784.
[8]. P. K. Verma, S. K. Singh, A. Kumar and S. Singh "Design and Analysis of Logic Gates Using Static and Domino Logic Technique", International Journal of Scientific & Technology Research, June 2012, Vol. 1, No. 5, pp. 122-125.
[9]. S. Jia, S. Lyu, Q. Meng, F. Wu and H. Xu, "A New Low-Power CMOS Dynamic Logic Circuit", IEEE conference on EDDSSC, 2013, Hong Kong.
[10]. K.S. Yeo, K. Roy, "Low- Voltage, Low-Power VLSI Subsystems".
[11]. H. F. Dadgour and K. Banerjee, "A Novel Variation-Tolerant Keeper Architecture for High-Performance Low-Power Wide Fan-In Dynamic OR Gates", IEEE Trans. on VLSI Systems, Nov. 2010, Vol. 18, No. 11, pp. 1567-1577.
[12]. H.T. Bui, Y. Wang and Y. Jiang, ―Design and analysis of low-power 10-transister full adders using XOR-XNOR gates,‖ IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process, Vol. 49, no. 1, pp. 25- 30, Jan. 2002.
[13]. N. Wesley and K. Eshraghian, "Principles of CMOS VLSI Design," 2nd ED., Addison Wesley
[14]. Analysis of Several 2:1 Multiplexer Circuits at 90nm and 45nm Technologies, Ila Gupta, Neha Arora, Prof. B.P. Singh, International Journal of Scientific and Research Publications, Volume 2, Issue 2, February 2012
[15]. Sumeer Goel, Mohammed A. Elgamel, Magdy A. Bayoumi, Yasser Hanafy, (2006) ―Design Methodologies for High-Performance Noise-Tolerant XOR-XNOR Circuits,‖ IEEE Transactions on Circuits and Systems- I, Vol. 53, No. 4, pp. 867-878.